AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

Claim 1 (Currently amended): A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polishing stopper layer over a surface of a semiconductor substrate;

(b) forming a trench in said semiconductor substrate by etching said stopper layer and said semiconductor substrate;

(c) forming a first liner insulating layer of silicon oxide over a surface of said semiconductor substrate exposed in said trench;

(d) forming a second liner insulating layer of silicon nitride in direct contact with said first liner insulating layer, said second liner insulating layer having a thickness of 20 nm or thicker;

(e) depositing an isolation layer of silicon oxide by plasma CVD, said isolation layer burying a recess defined by said second liner insulating layer;

(f) polishing and removing an unnecessary region of said isolation layer by using said stopper layer as a polishing stopper; ~~and~~

(g) etching said stopper layer; and

wherein said second liner insulating layer has a tensile stress of 1.2 GPa or larger.

Claim 2 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein said step (e) comprises:

(e1) depositing a third liner insulating layer of silicon oxide over said second liner insulating layer by plasma CVD at a first bias; and

(e2) depositing an isolation layer of silicon oxide by plasma CVD at a second bias higher than the first bias, said isolation layer burying a recess defined by said third liner insulating layer.

Claim 3 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein the first bias in said step (e1) is no bias.

Claim 4 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein said step (e1) includes a step of performing pre-heating at 400 °C to 450 °C and a next step of forming said third liner insulating layer of silicon oxide.

Claim 5 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein said step (e1) deposits said third liner insulating layer of silicon oxide by diode parallel plate plasma CVD.

Claim 6 (Original): The method of manufacturing a semiconductor device according to claim 2, wherein said step (e2) is executed by using an inductive coupling plasma CVD system.

Claim 7 (Original): The method of manufacturing a semiconductor device according to claim 1, further comprising after said step (d), the step of performing annealing at 1000 °C to 1150 °C.

Claim 8 (Cancelled)

Claim 9 (Original): The method of manufacturing a semiconductor device according to claim 1, wherein the plasma CVD is high density plasma CVD.

Claim 10 (Original): A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polishing stopper layer over a surface of a semiconductor substrate;

(b) forming a trench in said semiconductor substrate by etching said stopper layer and said semiconductor substrate;

(c) forming a first liner insulating layer of silicon oxide over a surface of said semiconductor substrate exposed in said trench;

(d) forming a second liner insulating layer of silicon nitride over said first liner insulating layer;

(e1) depositing a third liner insulating layer of silicon oxide over said second liner insulating layer by plasma CVD at a first bias;

(e2) depositing an isolation layer of silicon oxide by plasma CVD at a second bias higher than the first bias, said isolation layer burying a recess defined by said third liner insulating layer;

(f) polishing and removing an unnecessary region of said isolation layer by using said stopper layer as a polishing stopper; and

(g) etching said stopper layer.

Claim 11 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein the first bias in said step (e1) is no bias.

Claim 12 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said step (e1) includes a step of performing pre-heating at 400 °C to 450 °C and a next step of forming said third liner insulating layer of silicon oxide.

Claim 13 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said step (e1) deposits said third liner insulating layer of silicon oxide by diode parallel plate plasma CVD.

Claim 14 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said step (e2) is executed by using an inductive coupling plasma CVD system.

Claim 15 (Original): The method of manufacturing a semiconductor device according to claim 10, further comprising after said step (d), a step of performing annealing at 1000 °C to 1150 °C.

Claim 16 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein said second liner insulating layer has a tensile stress of 1.2 GPa or larger.

Claim 17 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein the plasma CVD is high density plasma CVD.

Claim 18 (Original): The method of manufacturing a semiconductor device according to claim 10, wherein the second liner insulating layer has a thickness of 8 nm or thinner.

Claim 19 (Currently amended): A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polishing stopper layer over a surface of a semiconductor substrate;

(b) forming a trench in said semiconductor substrate by etching said stopper layer and said semiconductor substrate;

(c) forming a first liner insulating layer of silicon oxide over a surface of said semiconductor substrate exposed in said trench;

(d) forming a second liner insulating layer of carbon-containing silicon nitride over said first liner insulating layer;

(e) depositing an isolation layer of silicon oxide by plasma CVD, said isolation layer burying a recess defined by said second liner insulating layer;

(f) polishing and removing an unnecessary region of said isolation layer by using said stopper layer as a polishing stopper; ~~and~~

(g) etching said stopper layer; and

wherein said second liner layer has a tensile stress larger than 1.2 GPa.

Claim 20 (Original): The method of manufacturing a semiconductor device according to claim 19, wherein said step (d) deposits the carbon-containing silicon nitride layer by chemical vapor deposition using organic silicon source gas, or a combination of silicon source gas and an organic gas.

Claim 21 (Original): The method of manufacturing a semiconductor device according to claim 19, wherein said step (d) deposits the carbon-containing silicon nitride layer by chemical vapor deposition using bis-tertial butylaminosilane (BTBAS) and ammonia as source gas.

Claim 22 (Original): The method of manufacturing a semiconductor device according to claim 21, wherein said step (d) is carried out at a substrate temperature of 550 °C - 580 °C.

Claim 23 (Original): The method of manufacturing a semiconductor device according to claim 19, wherein said step (g) is carried out under such condition that etching rate for the second liner insulating layer is smaller than etching rate for the silicon nitride layer of said stopper layer.

Claim 24 (Currently amended): A semiconductor device comprising:

a semiconductor substrate;

a trench formed in said semiconductor substrate, and defining active regions;

a first liner layer of silicon oxide covering surface of each said trench;

a second liner layer of carbon-containing silicon nitride formed over said first liner layer;

an isolation region of silicon oxide formed over said second liner layer and filling said trench; ~~and~~

a p-channel MOS transistor formed in one of said active regions; and

wherein said second liner layer has a tensile stress larger than 1.2 GPa.

Claim 25 (Cancelled).

Claim 26 (Original): The semiconductor device according to claim 24, wherein said second liner layer does not form a divot relative to surface of the semiconductor substrate.

Claim 27 (Original): The semiconductor device according to claim 24, further comprising an n-channel MOS transistor formed in another of said active regions, forming CMOS configuration with said p-channel MOS transistor.

Claim 28 (Original): The semiconductor device according to claim 24, further comprising:

interlevel insulating layers covering said CMOS configuration, and having low UV absorption coefficient;

multi-layer wiring formed in said interlevel insulating layers.

Claim 29 (Currently amended): A semiconductor device comprising:

a semiconductor substrate;

a trench formed in said semiconductor substrate, and defining active regions;

a first liner layer of silicon oxide covering surface of each said trench;

a second liner layer of silicon nitride formed over said first liner layer by using a source gas which leaves carbon in product silicon nitride;

an isolation region of silicon oxide formed over said second liner layer and filling said trench; ~~and~~

a p-channel MOS transistor formed in one of said active regions; and

wherein said second liner layer has a tensile stress larger than 1.2 GPa.

Claim 30 (Cancelled)

Claim 31 (Previously presented): The semiconductor device according to claim 29, wherein said second liner layer does not form a divot relative to surface of the semiconductor substrate.

Claim 32 (Previously presented): The semiconductor device according to claim 29, further comprising an n-channel MOS transistor formed in another of said active regions, forming CMOS configuration with said p-channel MOS transistor.

Claim 33 (Previously presented): The semiconductor device according to claim 29, further comprising:

interlevel insulating layers covering said CMOS configuration, and having low UV absorption coefficient;

multi-layer wiring formed in said interlevel insulating layers.

Claim 34 (Previously presented): The semiconductor device according to claim 24, wherein said source gas is BTBAS.

Claim 35 (Previously Presented): The method of manufacturing a semiconductor device according to claim 1, further comprising said second liner insulating layer having a thickness of greater than 20 nm.

Claim 36 (Previously presented): The method of manufacturing a semiconductor device according to claim 1, wherein the thickness of said second liner insulating layer is greater than 20nm.